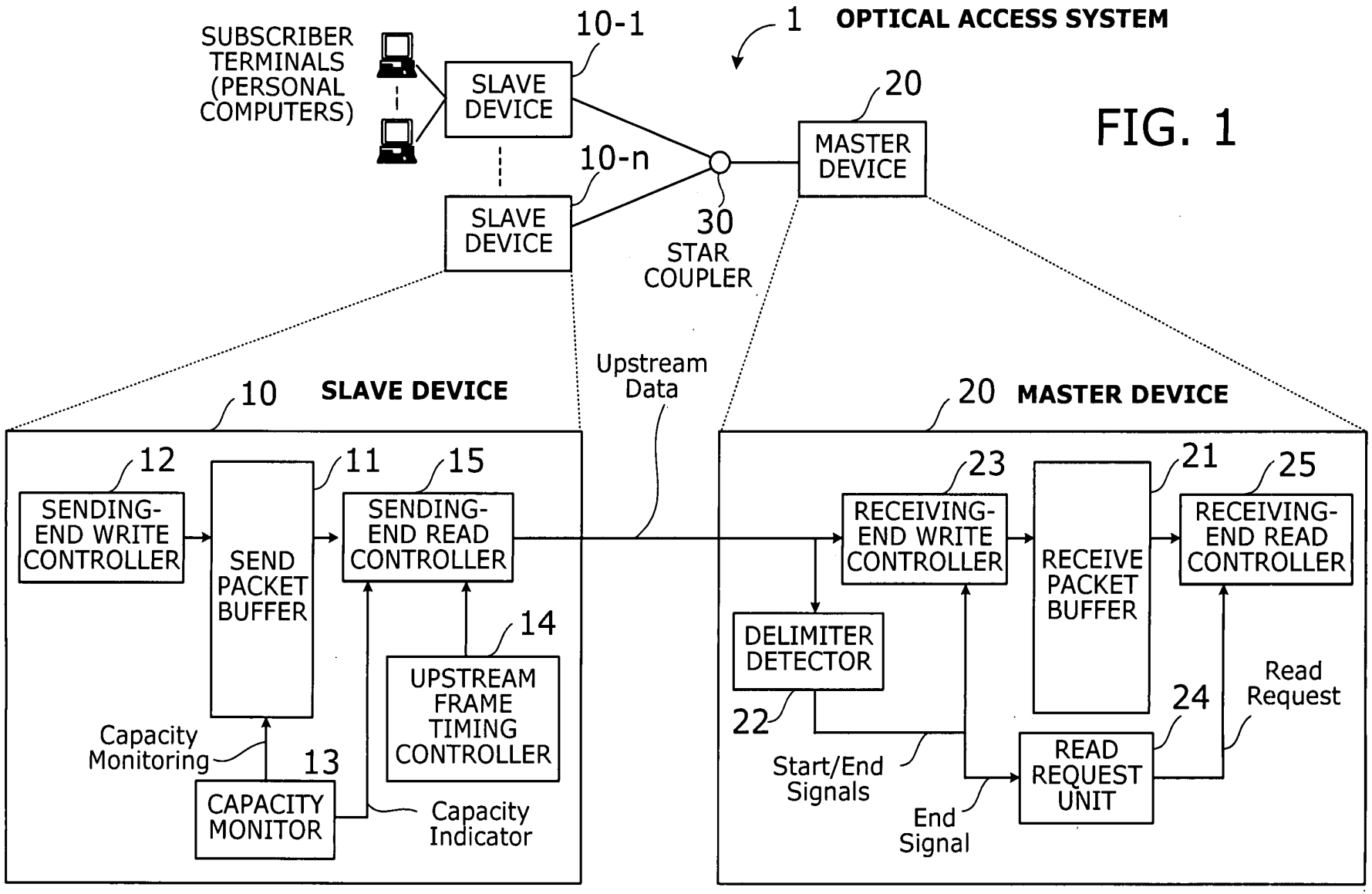

SUBSCRIBER TERMINALS (PERSONAL COMPUTERS)
10-1
SLAVE DEVICE
10-n
SLAVE DEVICE
1 OPTICAL ACCESS SYSTEM
20
MASTER DEVICE
30
STAR COUPLER
Upstream Data
10 SLAVE DEVICE
12
SENDING-END WRITE CONTROLLER
11
SEND PACKET BUFFER
15
SENDING-END READ CONTROLLER
14
UPSTREAM FRAME TIMING CONTROLLER
Capacity Monitoring
13
CAPACITY MONITOR
Capacity Indicator
20 MASTER DEVICE
23
RECEIVING-END WRITE CONTROLLER
21
RECEIVE PACKET BUFFER
25
RECEIVING-END READ CONTROLLER
DELIMITER DETECTOR
22
Start/End Signals
End Signal
24
READ REQUEST UNIT
Read Request

FIG. 1

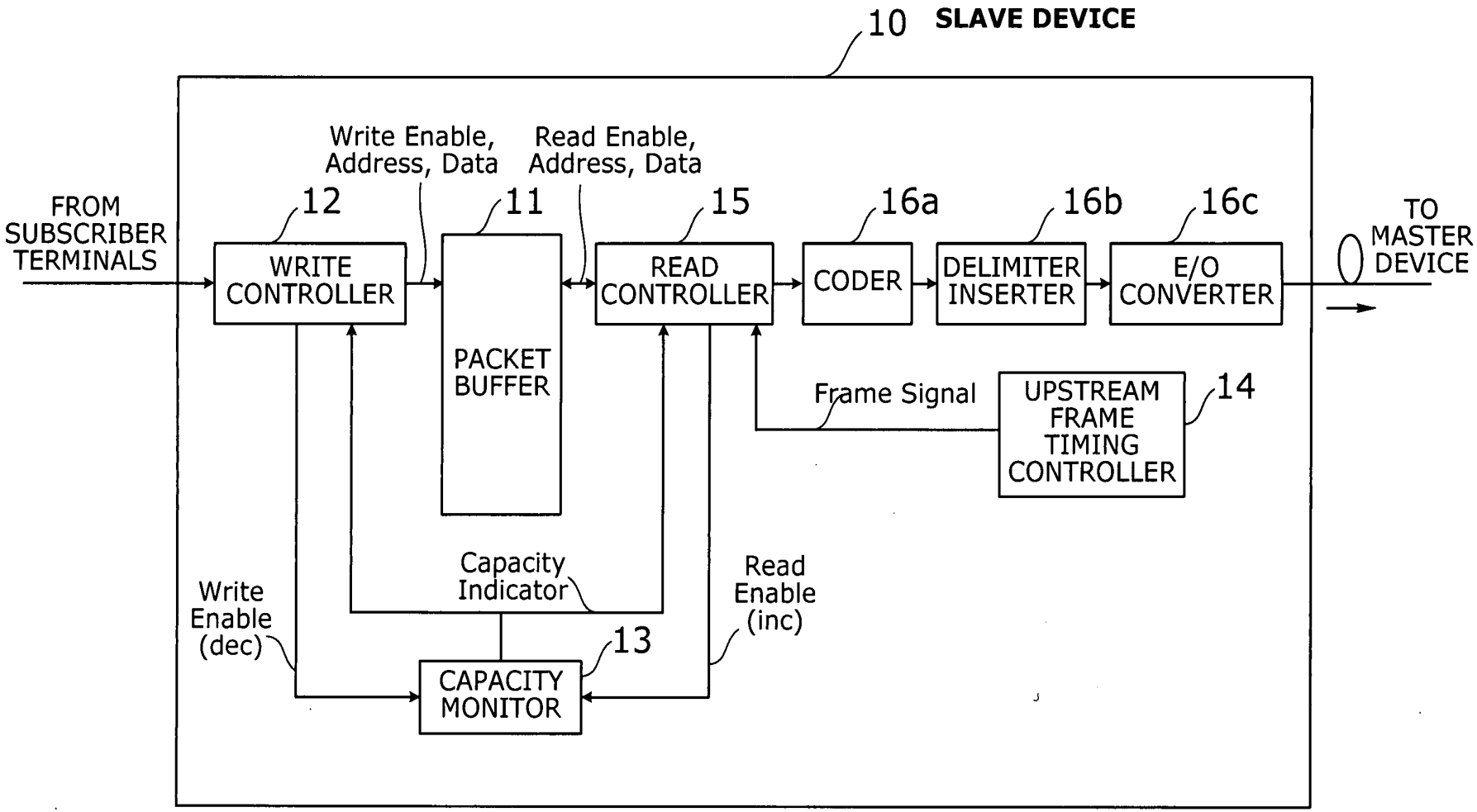

10 SLAVE DEVICE
Write Enable, Address, Data
Read Enable, Address, Data
FROM SUBSCRIBER TERMINALS
12
11
15
16a
16b
16c
WRITE CONTROLLER
PACKET BUFFER
READ CONTROLLER
CODER
DELIMITER INSERTER
E/O CONVERTER
TO MASTER DEVICE
Frame Signal
UPSTREAM FRAME TIMING CONTROLLER
14
Capacity Indicator
Write Enable (dec)
Read Enable (inc)
13
CAPACITY MONITOR

FIG. 2

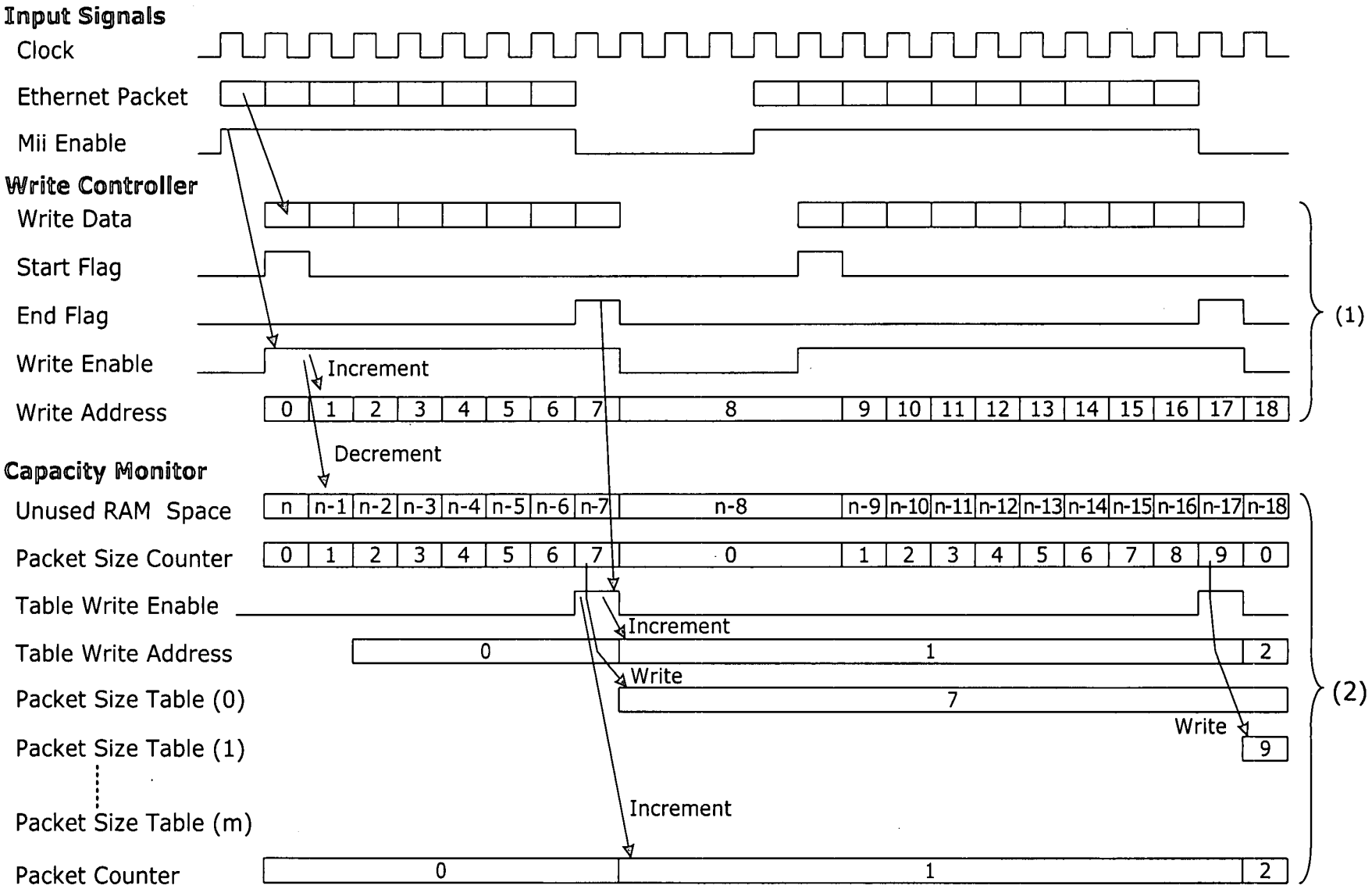

Input Signals
Clock
Ethernet Packet
Mii Enable
Write Controller
Write Data
Start Flag
End Flag
Write Enable
Write Address
Increment
Decrement
Capacity Monitor
Unused RAM Space
Packet Size Counter
Table Write Enable
Table Write Address
Packet Size Table (0)
Packet Size Table (1)
Packet Size Table (m)
Packet Counter
Increment
Write
Write
Increment
(1)
(2)
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
n n-1 n-2 n-3 n-4 n-5 n-6 n-7 n-8 n-9 n-10 n-11 n-12 n-13 n-14 n-15 n-16 n-17 n-18
0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 8 9 0
0 1 2
7
9
0 1 2

FIG. 3

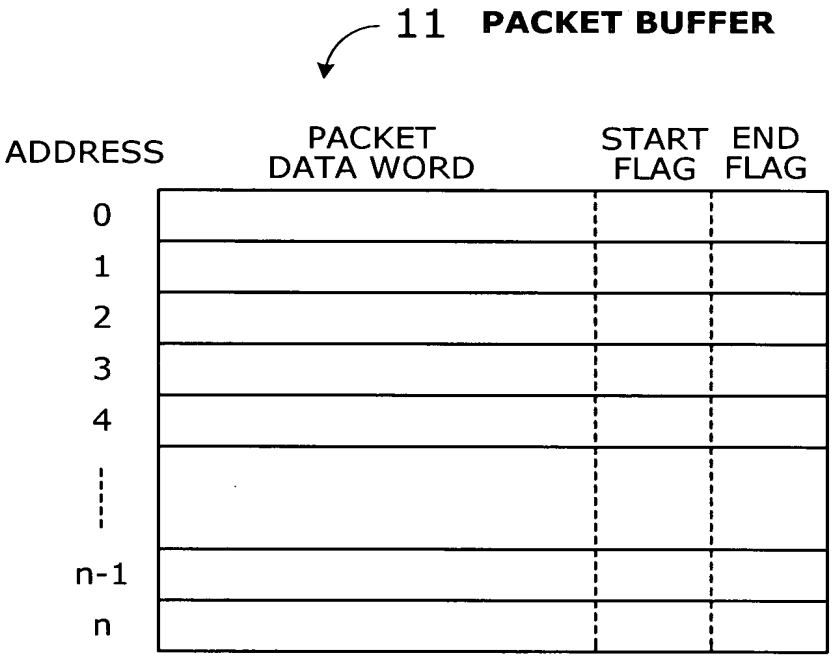

11
PACKET BUFFER
ADDRESS
PACKET DATA WORD
START FLAG
END FLAG
0
1
2
3
4
n-1
n

FIG. 4

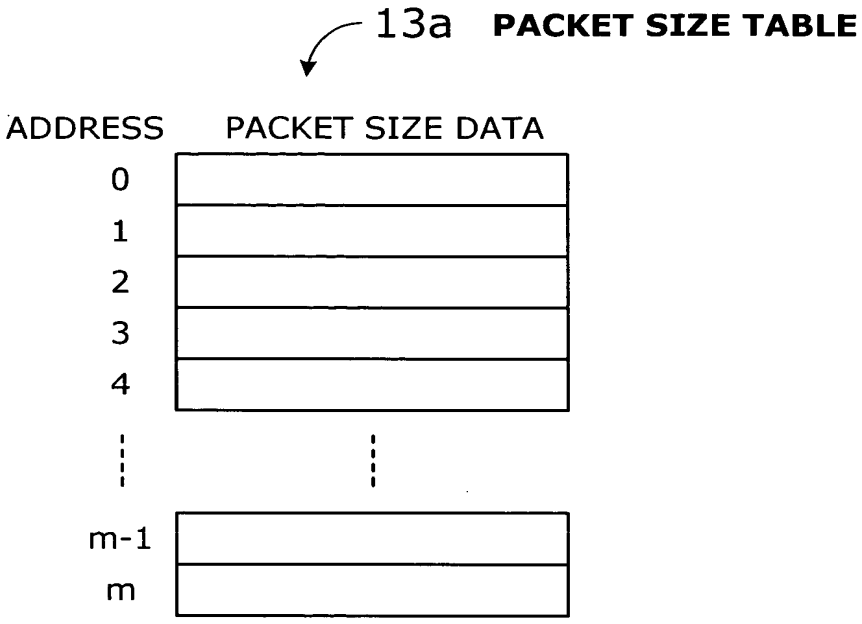


FIG. 5

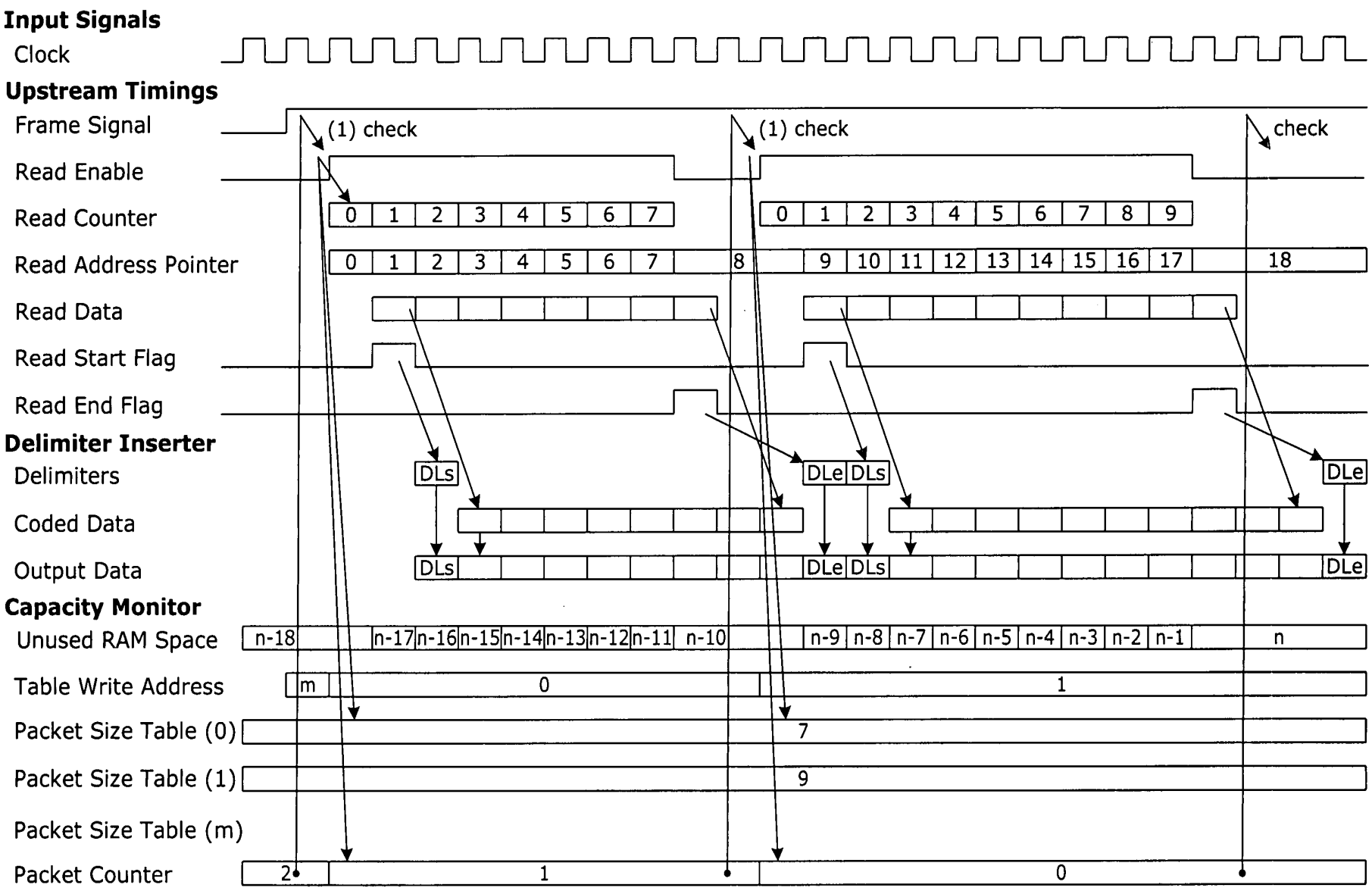

Input Signals
Clock
Upstream Timings
Frame Signal
Read Enable
Read Counter
Read Address Pointer
Read Data
Read Start Flag
Read End Flag
Delimiter Inserter
Delimiters
Coded Data
Output Data
Capacity Monitor
Unused RAM Space
Table Write Address
Packet Size Table (0)
Packet Size Table (1)
Packet Size Table (m)
Packet Counter
(1) check
(1) check
check
0 1 2 3 4 5 6 7
0 1 2 3 4 5 6 7 8 9
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
DLs
DLe DLs
DLe
n-18 n-17 n-16 n-15 n-14 n-13 n-12 n-11 n-10 n-9 n-8 n-7 n-6 n-5 n-4 n-3 n-2 n-1 n
m 0 1
7
9
2 1 0

FIG. 6

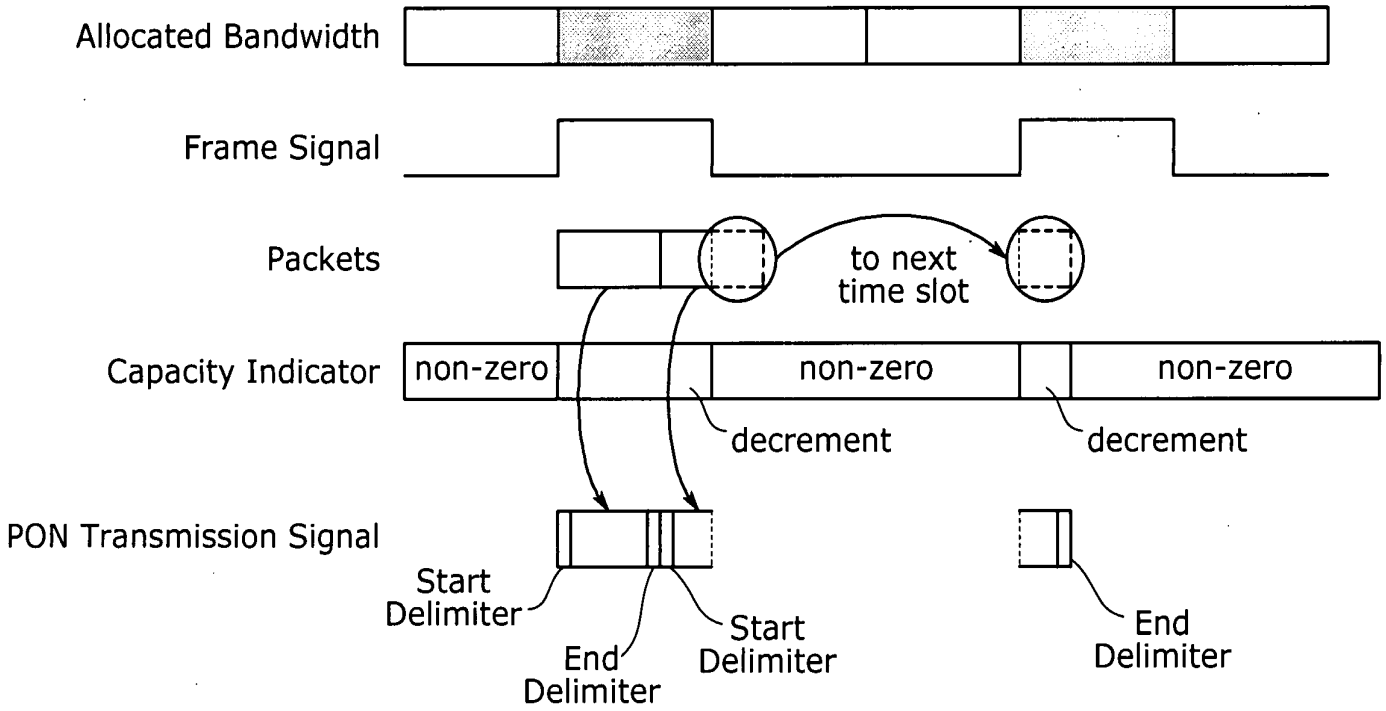

Allocated Bandwidth
Frame Signal
Packets
to next
time slot
Capacity Indicator
non-zero
non-zero
non-zero
decrement
decrement
PON Transmission Signal
Start
Delimiter
End
Delimiter
Start
Delimiter
End
Delimiter

FIG. 7

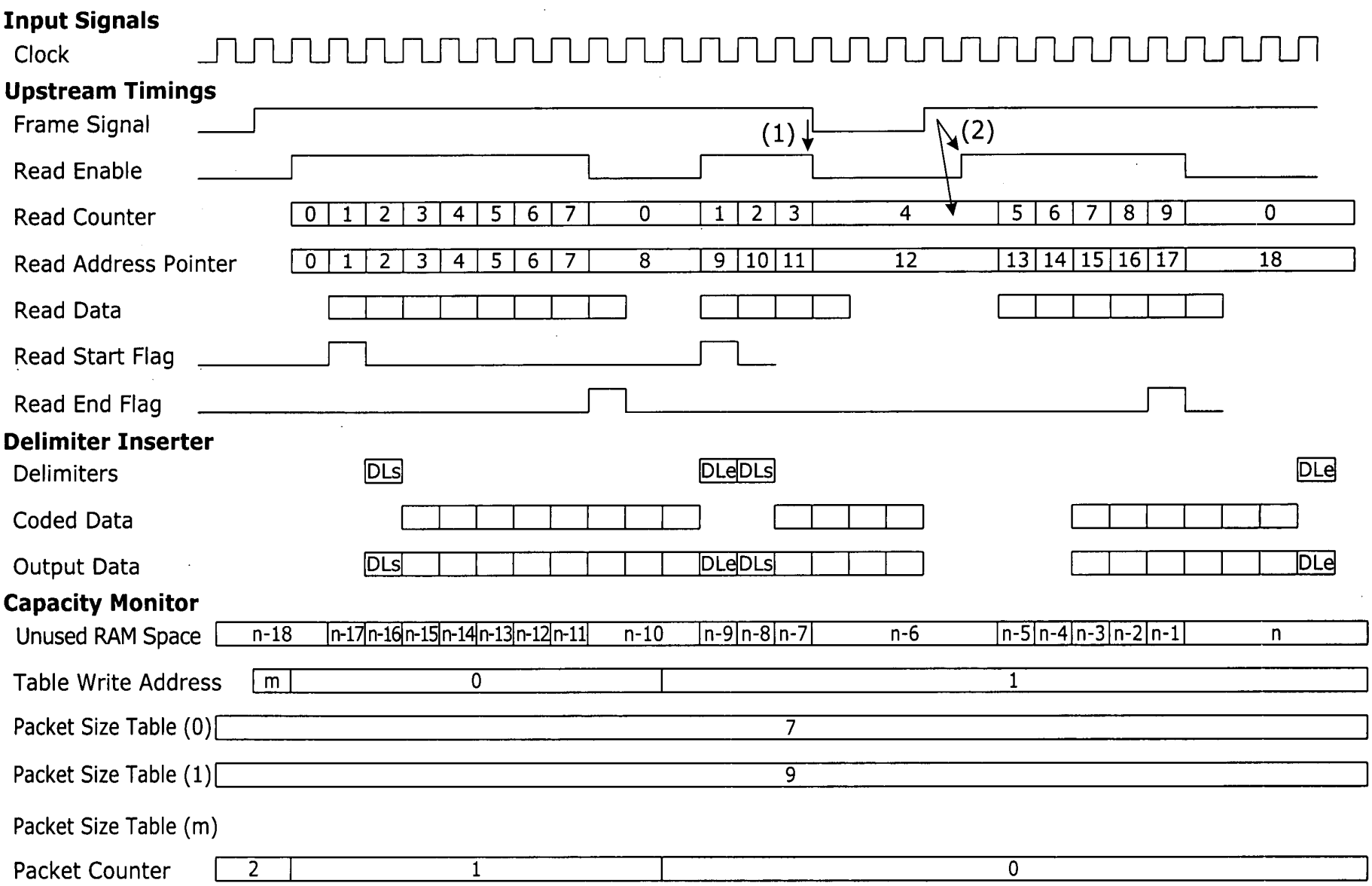

Input Signals
Clock
Upstream Timings
Frame Signal
(1)
(2)
Read Enable
Read Counter
0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 8 9 0
Read Address Pointer
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
Read Data
Read Start Flag
Read End Flag
Delimiter Inserter
Delimiters
DLs
DLe DLs
DLe
Coded Data
Output Data
DLs
DLe DLs
DLe
Capacity Monitor
Unused RAM Space
n-18 n-17 n-16 n-15 n-14 n-13 n-12 n-11 n-10 n-9 n-8 n-7 n-6 n-5 n-4 n-3 n-2 n-1 n
Table Write Address
m 0 1
Packet Size Table (0)
7
Packet Size Table (1)
9
Packet Size Table (m)
Packet Counter
2 1 0

FIG. 8

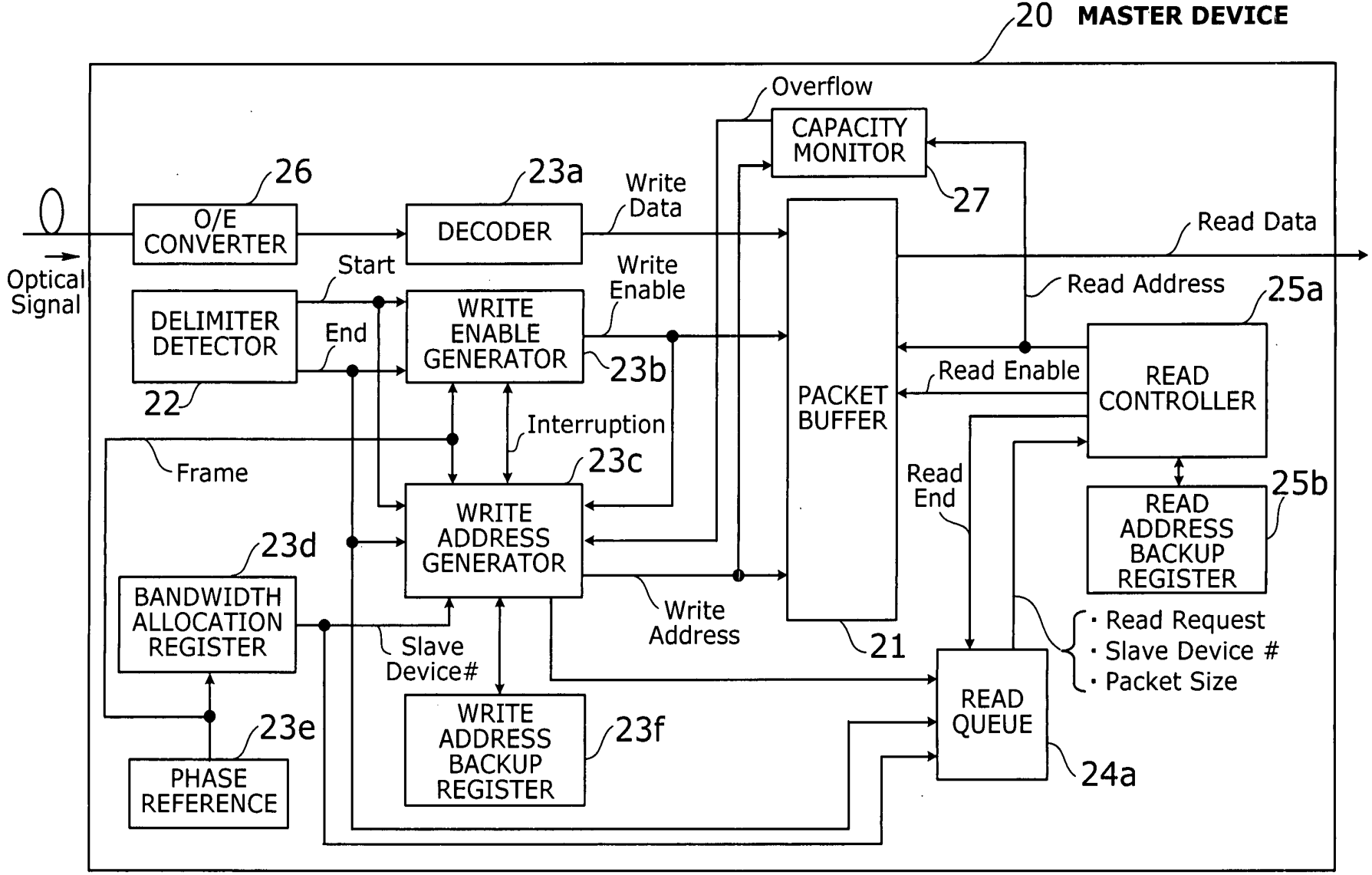

20 MASTER DEVICE
Optical Signal
26
O/E CONVERTER
23a
DECODER
Write Data
Overflow
CAPACITY MONITOR
27
Read Data
Start
End
DELIMITER DETECTOR
22
WRITE ENABLE GENERATOR
23b
Write Enable
Read Address
25a
PACKET BUFFER
Read Enable
READ CONTROLLER
Interruption
Frame
23c
Read End
25b
READ ADDRESS BACKUP REGISTER
WRITE ADDRESS GENERATOR
23d
BANDWIDTH ALLOCATION REGISTER
Write Address
21
Slave Device#
· Read Request
· Slave Device #
· Packet Size
READ QUEUE
24a
WRITE ADDRESS BACKUP REGISTER
23f
23e
PHASE REFERENCE

FIG. 9

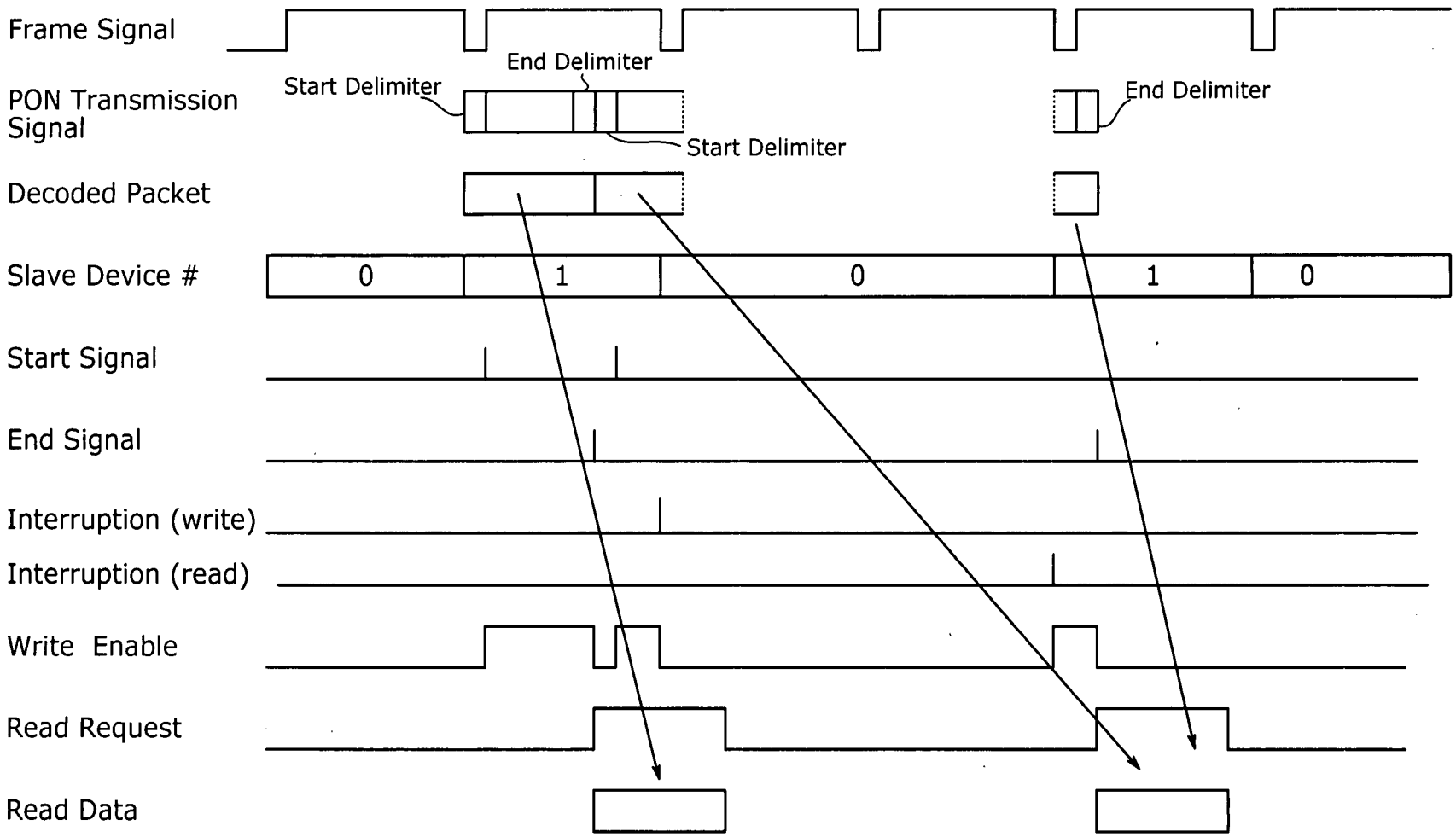

Frame Signal
PON Transmission Signal
Start Delimiter
End Delimiter
Start Delimiter
End Delimiter
Decoded Packet
Slave Device #
0
1
0
1
0
Start Signal
End Signal
Interruption (write)
Interruption (read)
Write Enable
Read Request
Read Data

FIG. 10

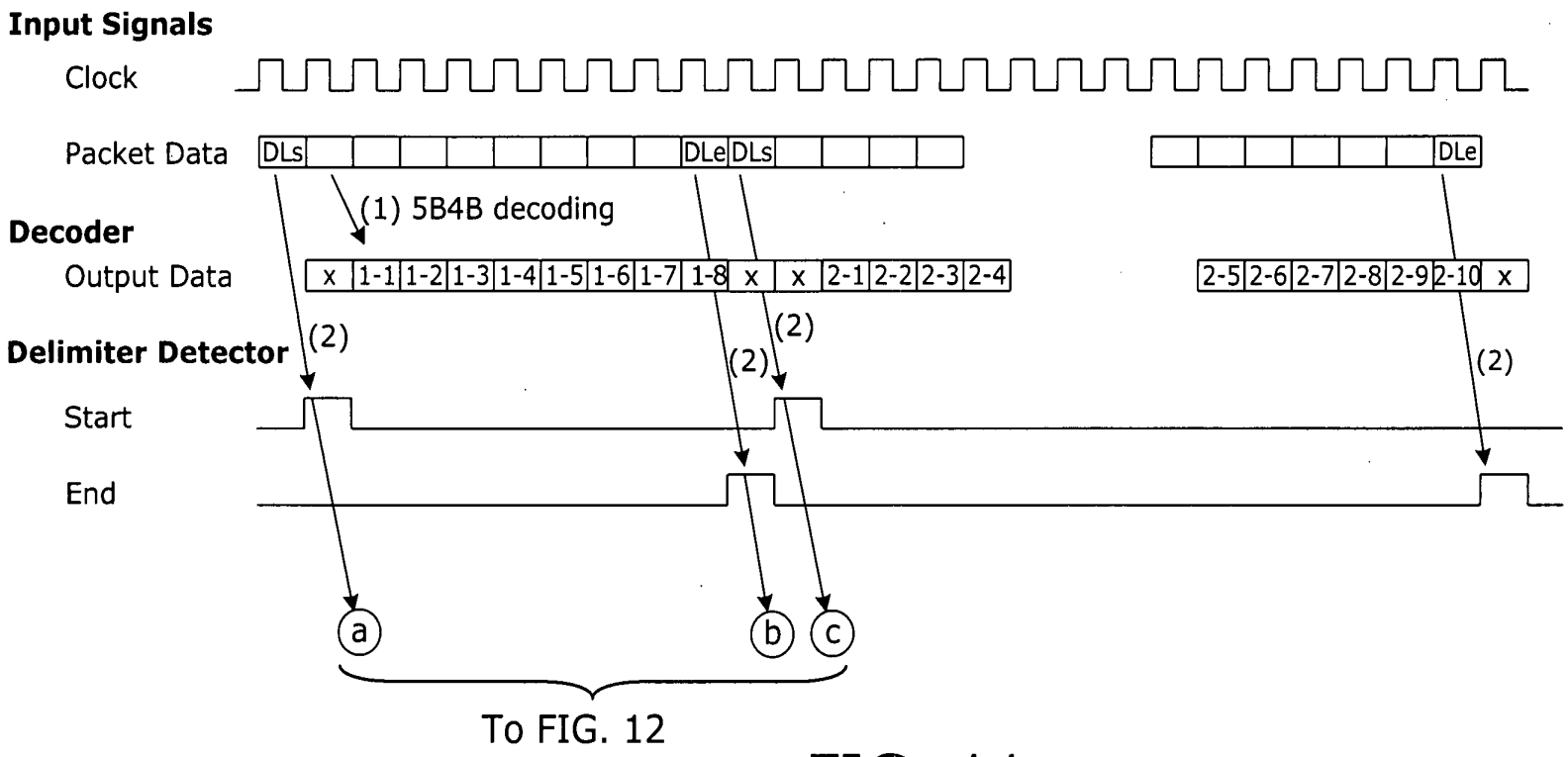

Input Signals
Clock
Packet Data
DLs
DLe
DLs
DLe
(1) 5B4B decoding
Decoder
Output Data
x
1-1
1-2
1-3
1-4
1-5
1-6
1-7
1-8
x
x
2-1
2-2
2-3
2-4
2-5
2-6
2-7
2-8
2-9
2-10
x
Delimiter Detector
(2)
(2)
(2)
(2)
Start
End
a
b
c
To FIG. 12

FIG. 11

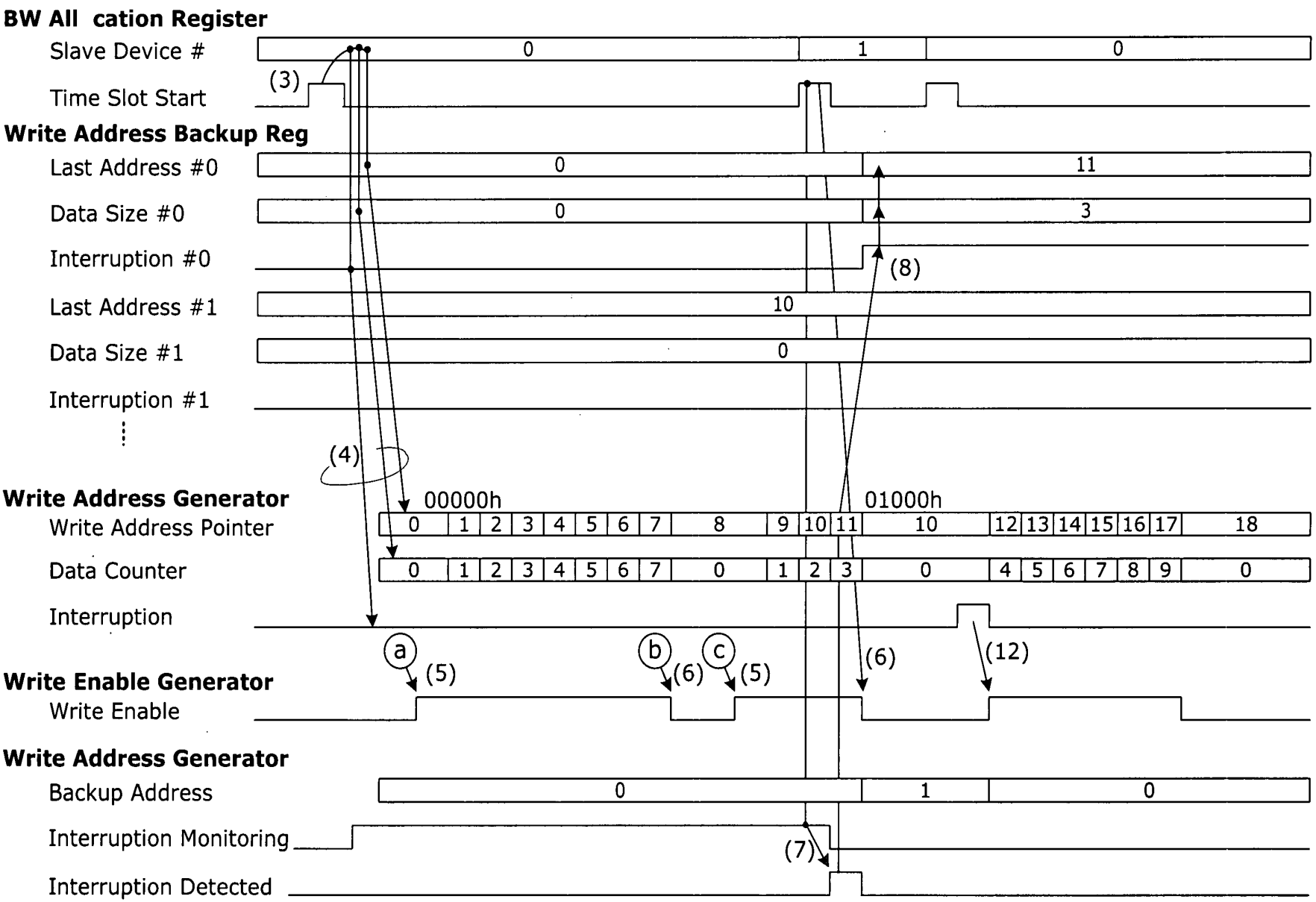

BW All cation Register
Slave Device #
Time Slot Start
(3)
Write Address Backup Reg
Last Address #0
Data Size #0
Interruption #0
Last Address #1
Data Size #1
Interruption #1
(4)
Write Address Generator
Write Address Pointer
Data Counter
Interruption
00000h
01000h
(8)
a
b
c
(5)
(6)
(5)
(6)
(12)
Write Enable Generator
Write Enable
Write Address Generator
Backup Address
Interruption Monitoring
(7)
Interruption Detected

FIG. 12

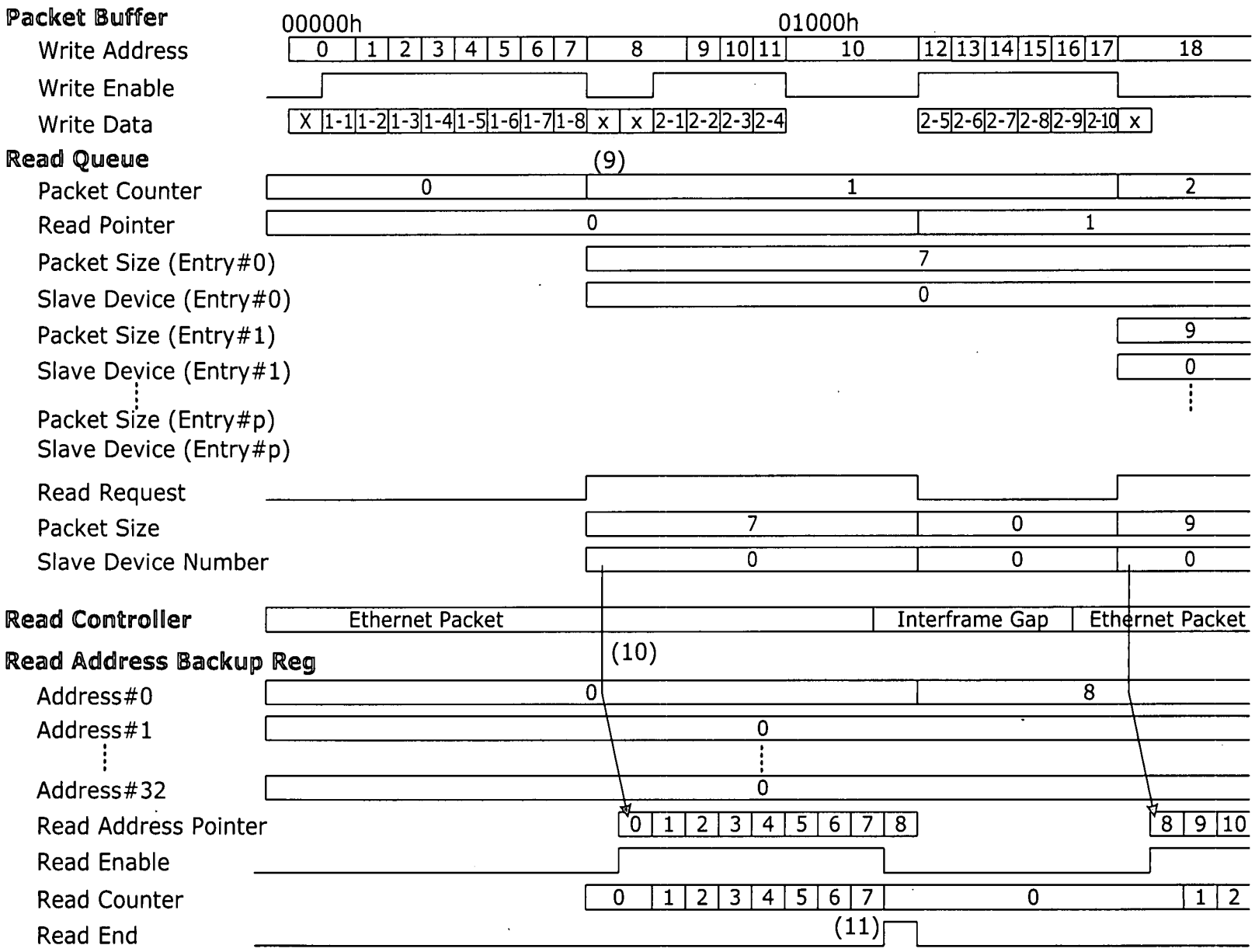

Packet Buffer
00000h
01000h
Write Address
Write Enable
Write Data
Read Queue
(9)
Packet Counter
Read Pointer
Packet Size (Entry#0)
Slave Device (Entry#0)
Packet Size (Entry#1)
Slave Device (Entry#1)
Packet Size (Entry#p)
Slave Device (Entry#p)
Read Request
Packet Size
Slave Device Number
Read Controller
Ethernet Packet
Interframe Gap
Ethernet Packet
Read Address Backup Reg
(10)
Address#0
Address#1
Address#32
Read Address Pointer
Read Enable
Read Counter
Read End
(11)

FIG. 13

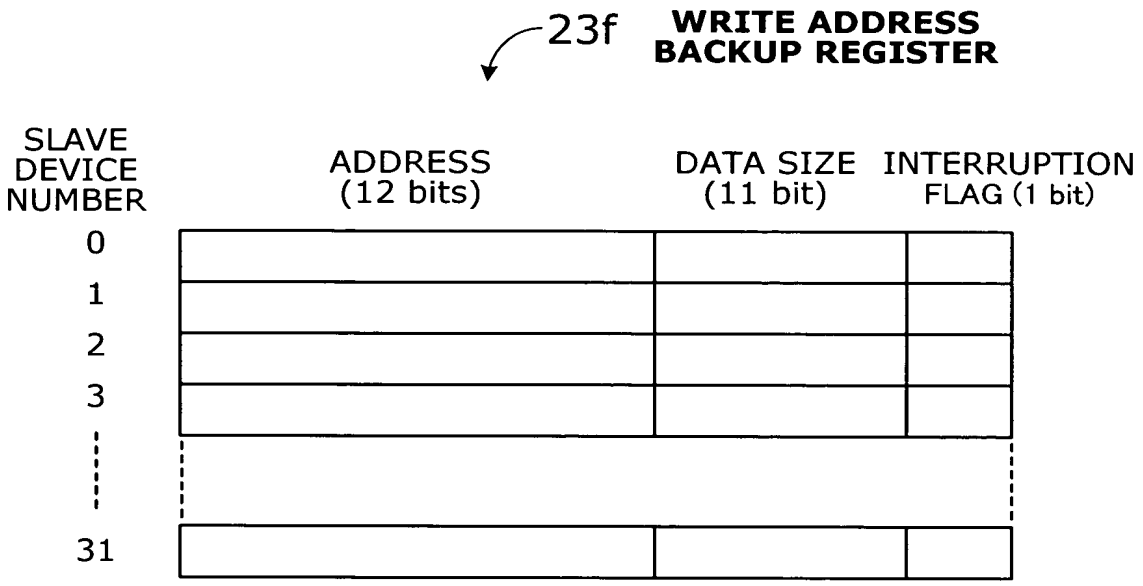

23f
WRITE ADDRESS BACKUP REGISTER
SLAVE DEVICE NUMBER
ADDRESS (12 bits)
DATA SIZE (11 bit)
INTERRUPTION FLAG (1 bit)
0
1
2
3
31

FIG. 14

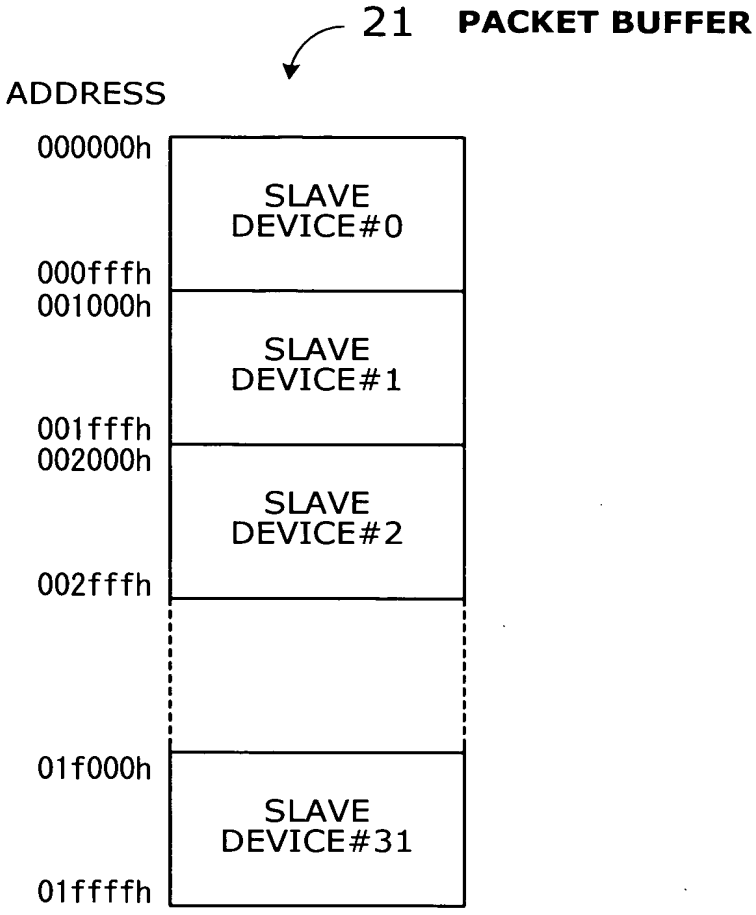

21
PACKET BUFFER
ADDRESS
000000h
SLAVE DEVICE#0
000fffh
001000h
SLAVE DEVICE#1
001fffh
002000h
SLAVE DEVICE#2
002fffh
01f000h
SLAVE DEVICE#31
01ffffh

FIG. 15

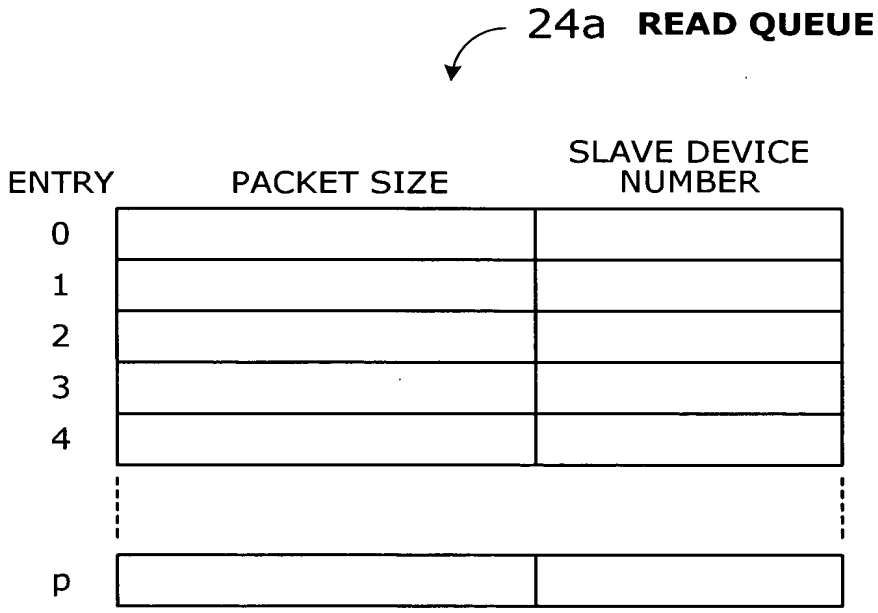
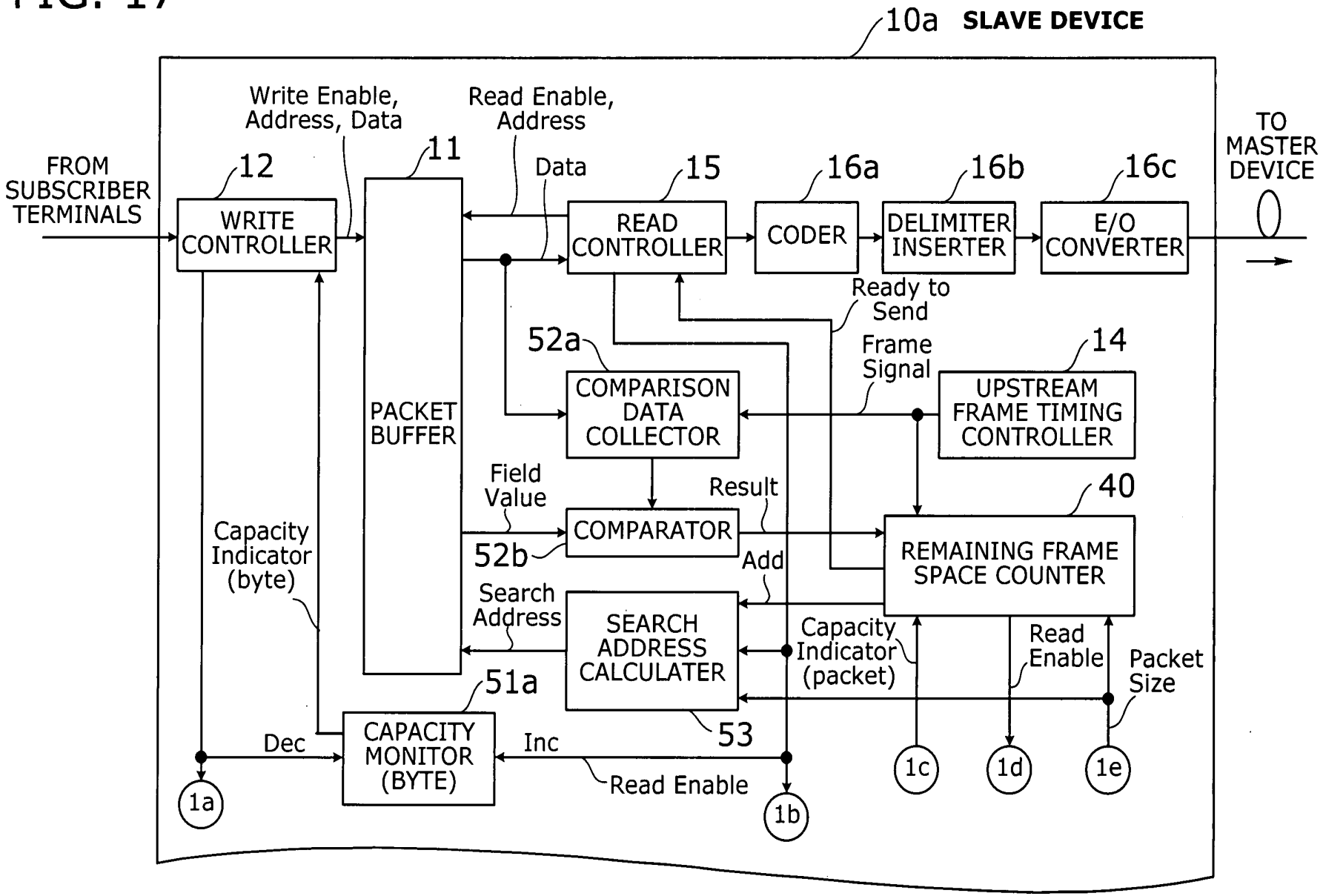

24a READ QUEUE
ENTRY
PACKET SIZE
SLAVE DEVICE NUMBER
0
1
2
3
4
p

FIG. 16

FIG. 17


10a SLAVE DEVICE
FROM SUBSCRIBER TERMINALS
Write Enable, Address, Data
Read Enable, Address
Data
12
11
15
16a
16b
16c
TO MASTER DEVICE
WRITE CONTROLLER
PACKET BUFFER
READ CONTROLLER
CODER
DELIMITER INSERTER
E/O CONVERTER
Ready to Send
52a
Frame Signal
14
COMPARISON DATA COLLECTOR
UPSTREAM FRAME TIMING CONTROLLER
Field Value
Result
40
Capacity Indicator (byte)
COMPARATOR
52b
Add
REMAINING FRAME SPACE COUNTER
Search Address
SEARCH ADDRESS CALCULATER
Capacity Indicator (packet)
Read Enable
Packet Size
51a
53
Dec
CAPACITY MONITOR (BYTE)
Inc
Read Enable
1a
1b
1c
1d
1e

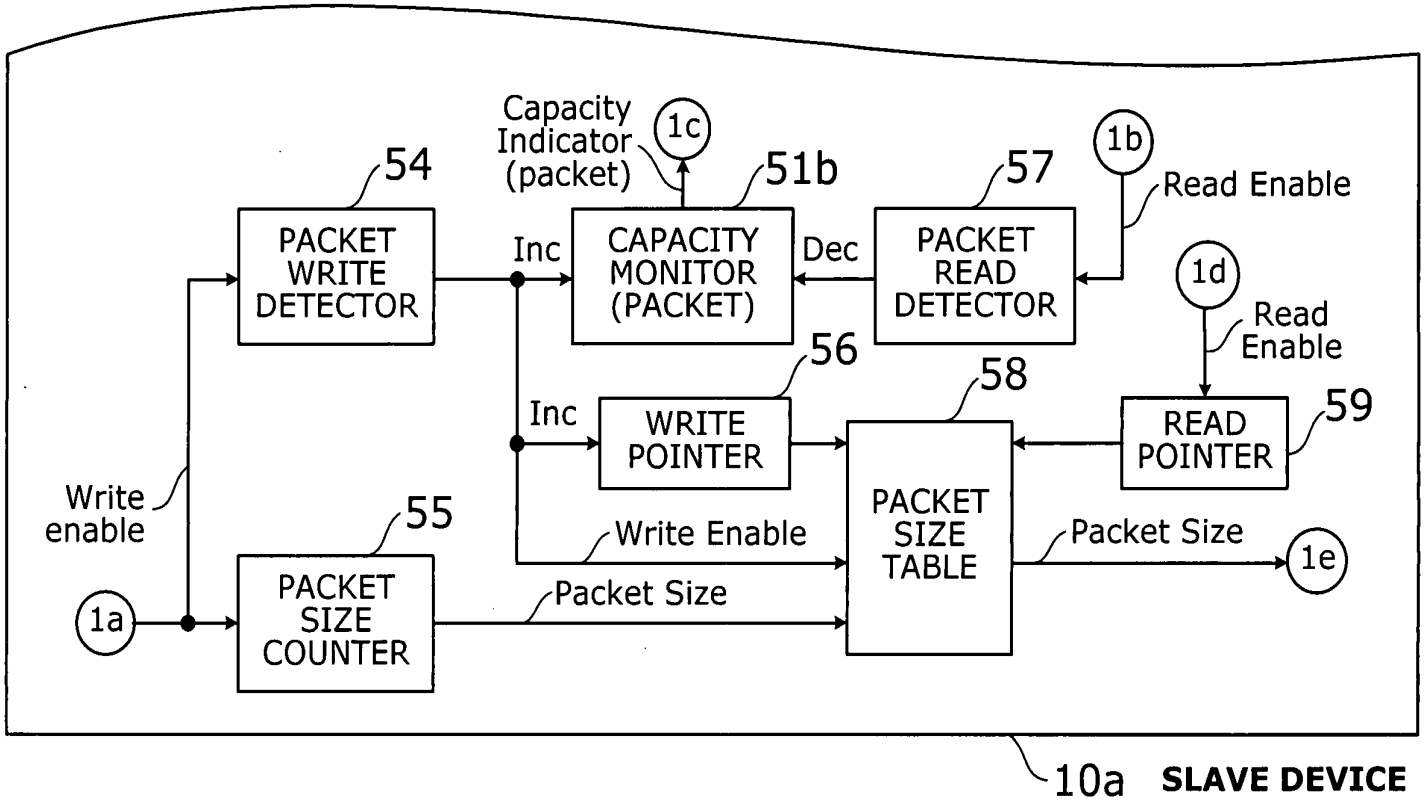

Capacity
Indicator
(packet)
1c
54
51b
57
1b
Read Enable
PACKET
WRITE
DETECTOR
Inc
CAPACITY
MONITOR
(PACKET)
Dec
PACKET
READ
DETECTOR
1d
Read
Enable
56
58
59
Inc
WRITE
POINTER
READ
POINTER
Write
enable
55
PACKET
SIZE
TABLE
Write Enable
Packet Size
1e
1a
PACKET
SIZE
COUNTER
Packet Size
10a
SLAVE DEVICE

FIG. 18

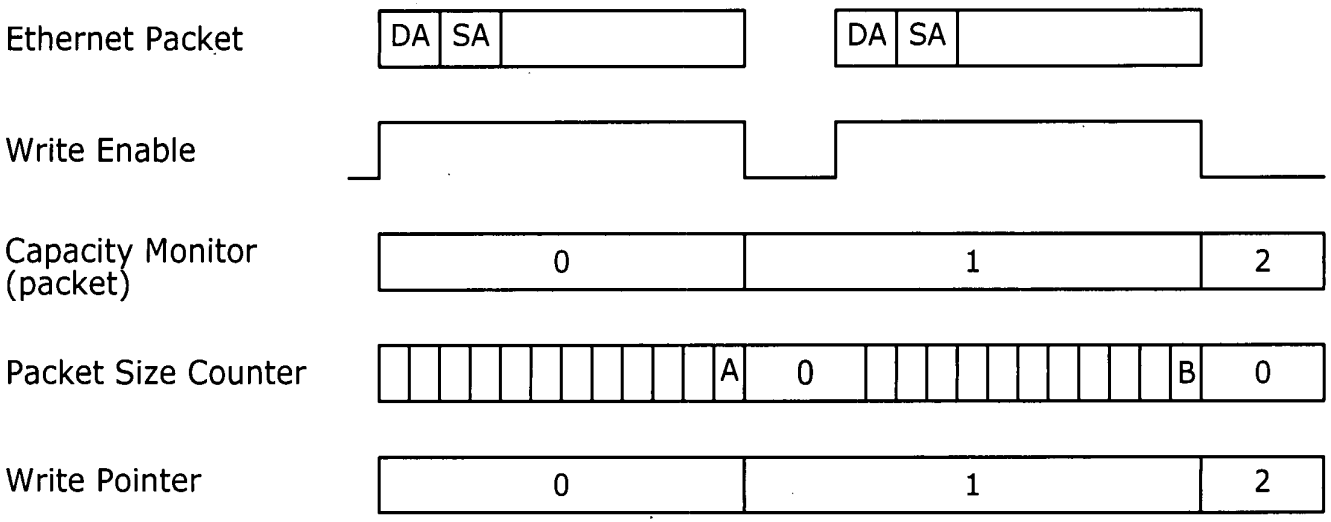

Ethernet Packet
DA
SA
DA
SA
Write Enable
Capacity Monitor (packet)
0
1
2
Packet Size Counter
A
0
B
0
Write Pointer
0
1
2

FIG. 19

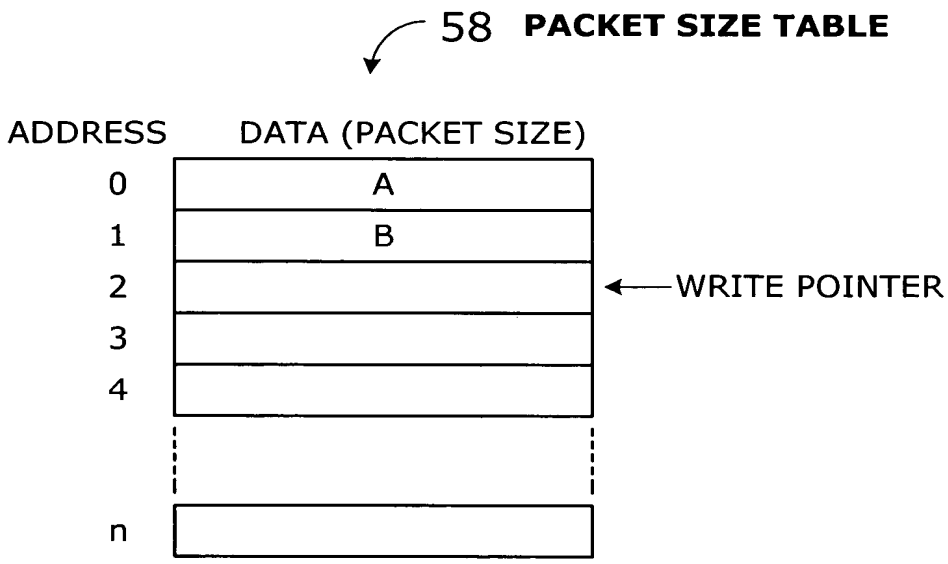

58 PACKET SIZE TABLE
ADDRESS
DATA (PACKET SIZE)
0
A
1
B
2
WRITE POINTER
3
4
n

FIG. 20

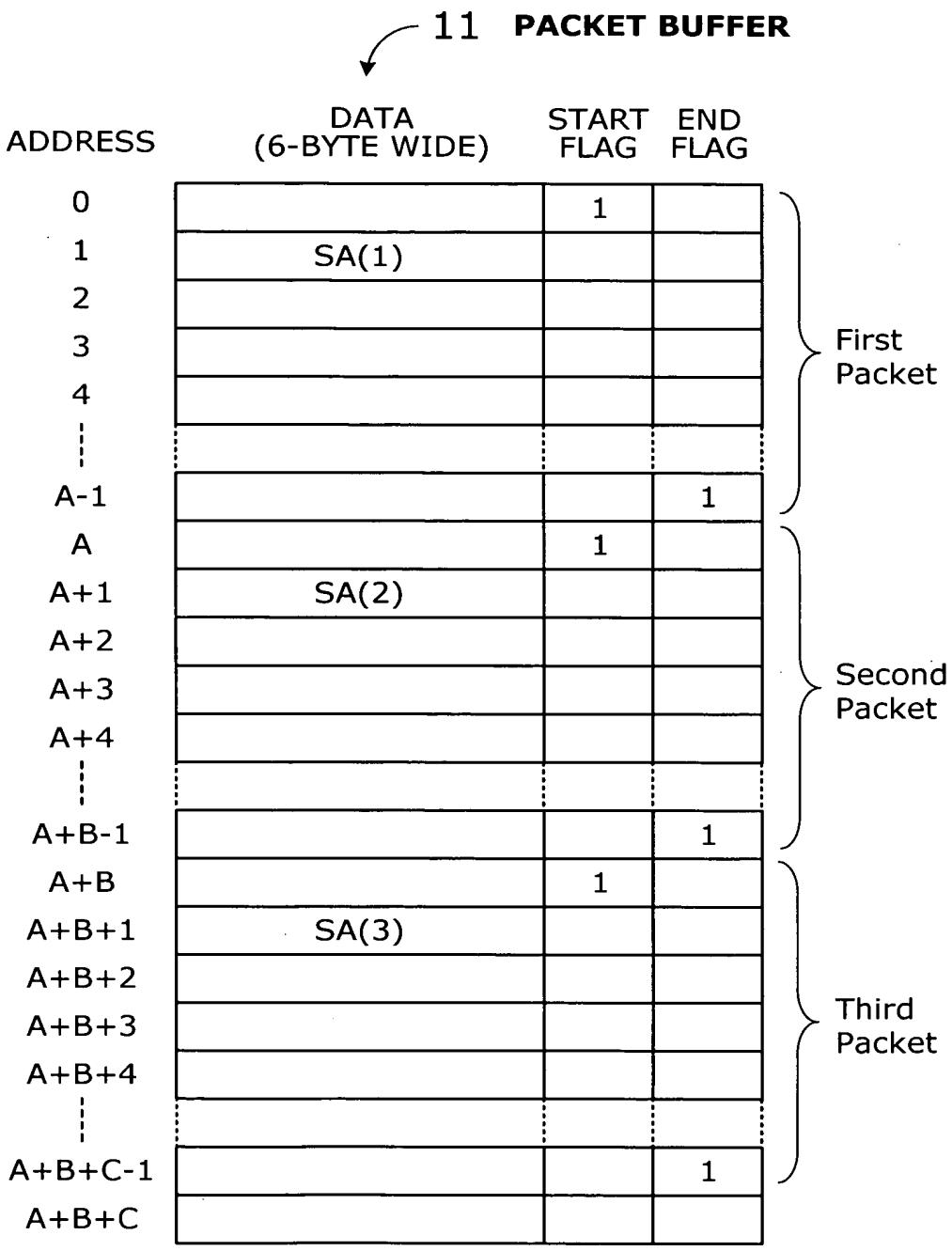

11 PACKET BUFFER
ADDRESS
DATA (6-BYTE WIDE)
START FLAG
END FLAG
0
1
SA(1)
2
3
4
A-1
1
First Packet
A
1
A+1
SA(2)
A+2
A+3
A+4
A+B-1
1
Second Packet
A+B
1
A+B+1
SA(3)
A+B+2
A+B+3
A+B+4
A+B+C-1
1
Third Packet
A+B+C

FIG. 21

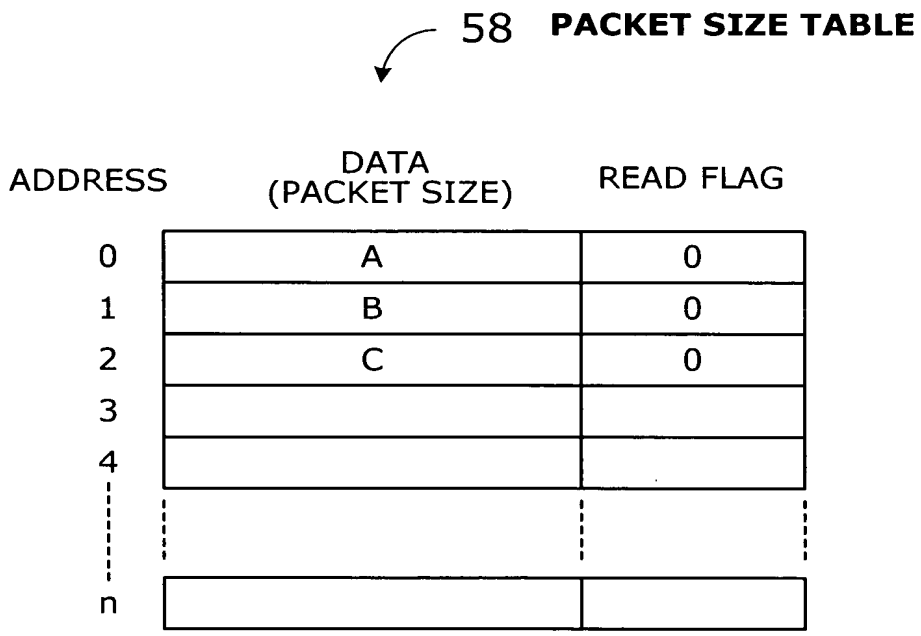

58
PACKET SIZE TABLE
ADDRESS
DATA
(PACKET SIZE)
READ FLAG
0
A
0
1
B
0
2
C
0
3
4
n

FIG. 22

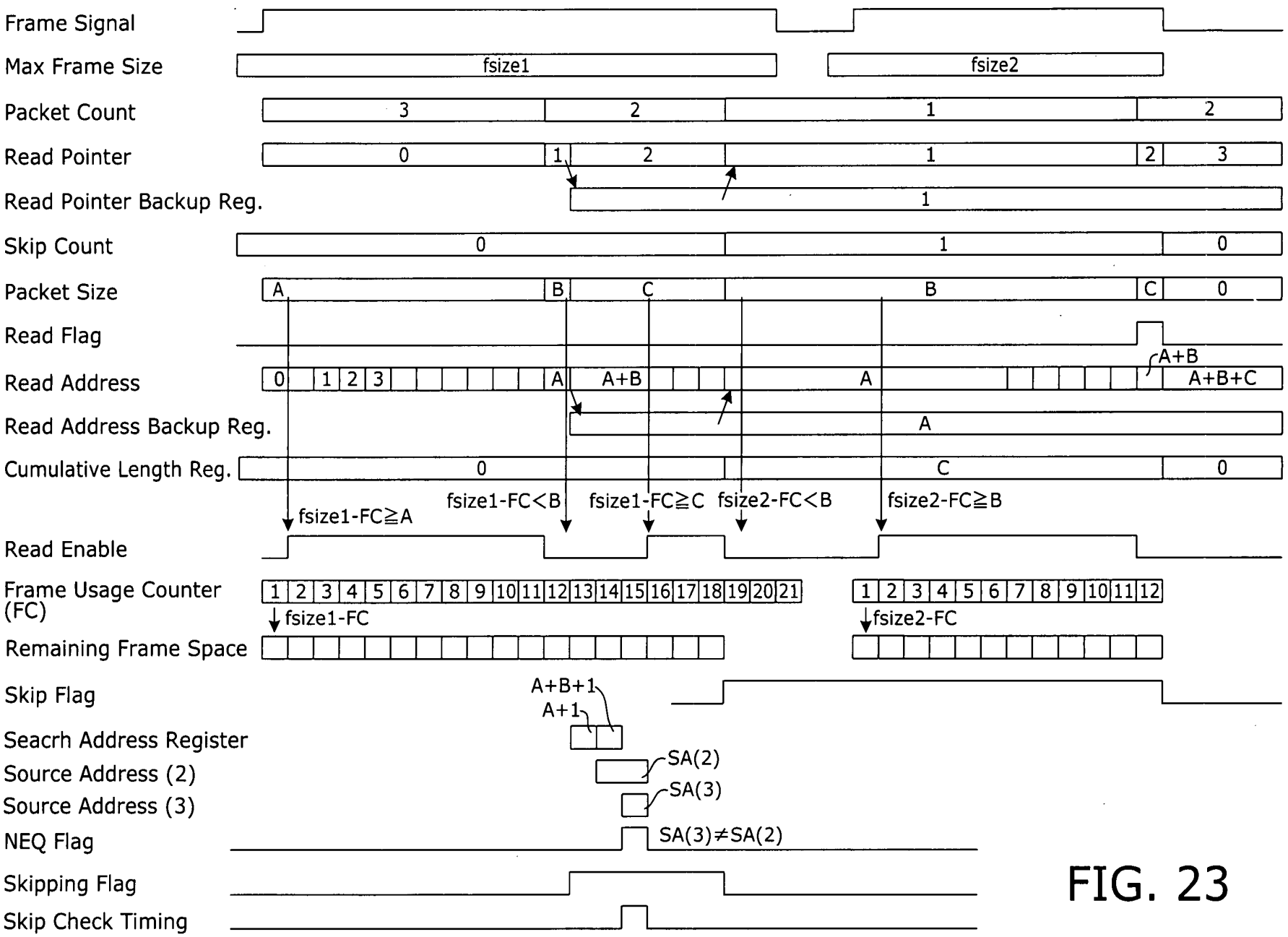

Frame Signal
Max Frame Size
fsize1
fsize2
Packet Count
Read Pointer
Read Pointer Backup Reg.
Skip Count
Packet Size
Read Flag
Read Address
Read Address Backup Reg.
Cumulative Length Reg.
fsize1-FC≧A
fsize1-FC<B
fsize1-FC≧C
fsize2-FC<B
fsize2-FC≧B
Read Enable
Frame Usage Counter (FC)
fsize1-FC
fsize2-FC
Remaining Frame Space
Skip Flag
A+B+1
A+1
Seacrh Address Register
Source Address (2)
SA(2)
Source Address (3)
SA(3)
NEQ Flag
SA(3)≠SA(2)
Skipping Flag
Skip Check Timing

FIG. 23

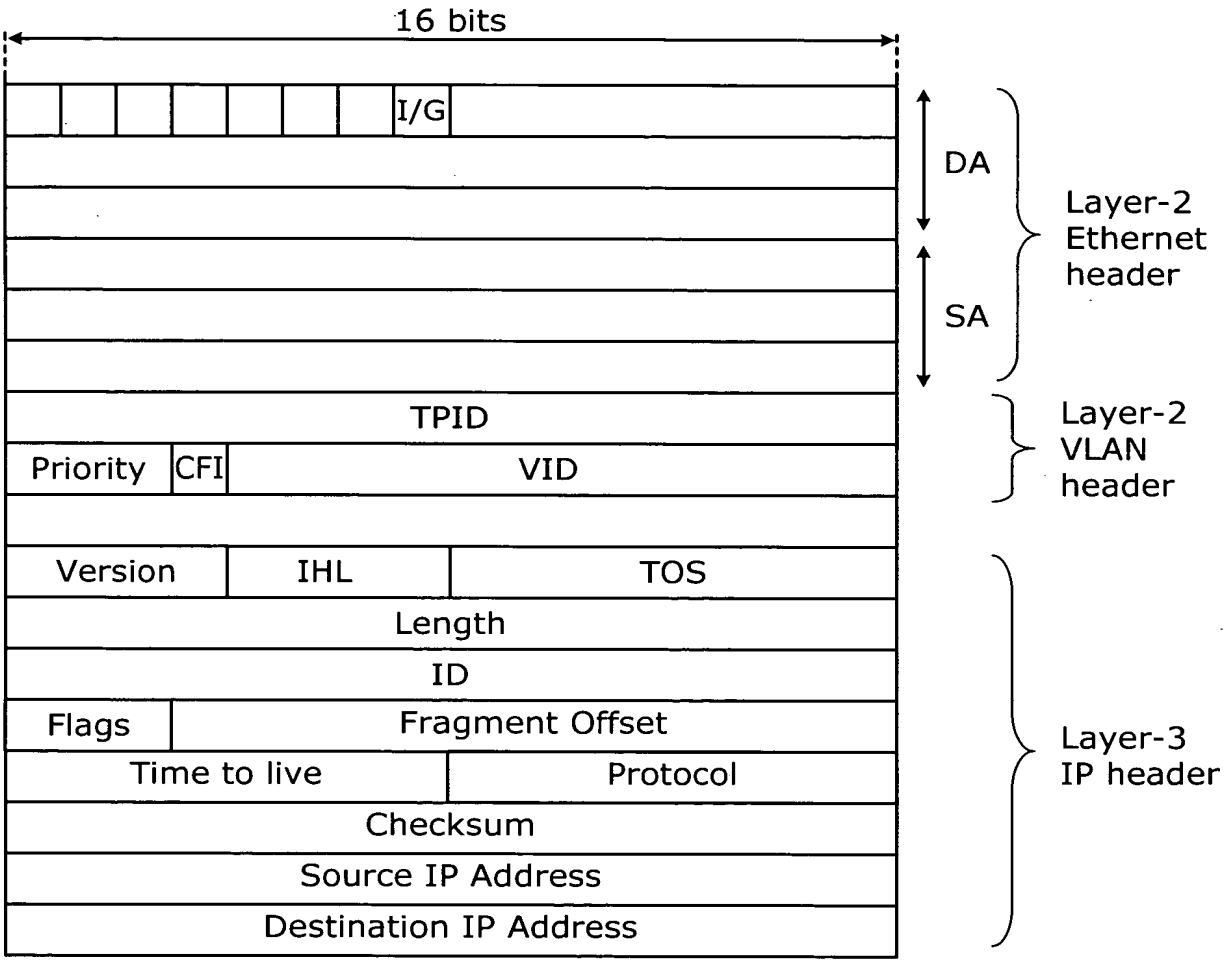

16 bits
I/G
DA
SA
Layer-2
Ethernet
header
TPID
Priority
CFI
VID
Layer-2
VLAN
header
Version
IHL
TOS
Length
ID
Flags
Fragment Offset
Time to live
Protocol
Checksum
Source IP Address
Destination IP Address
Layer-3
IP header

FIG. 24

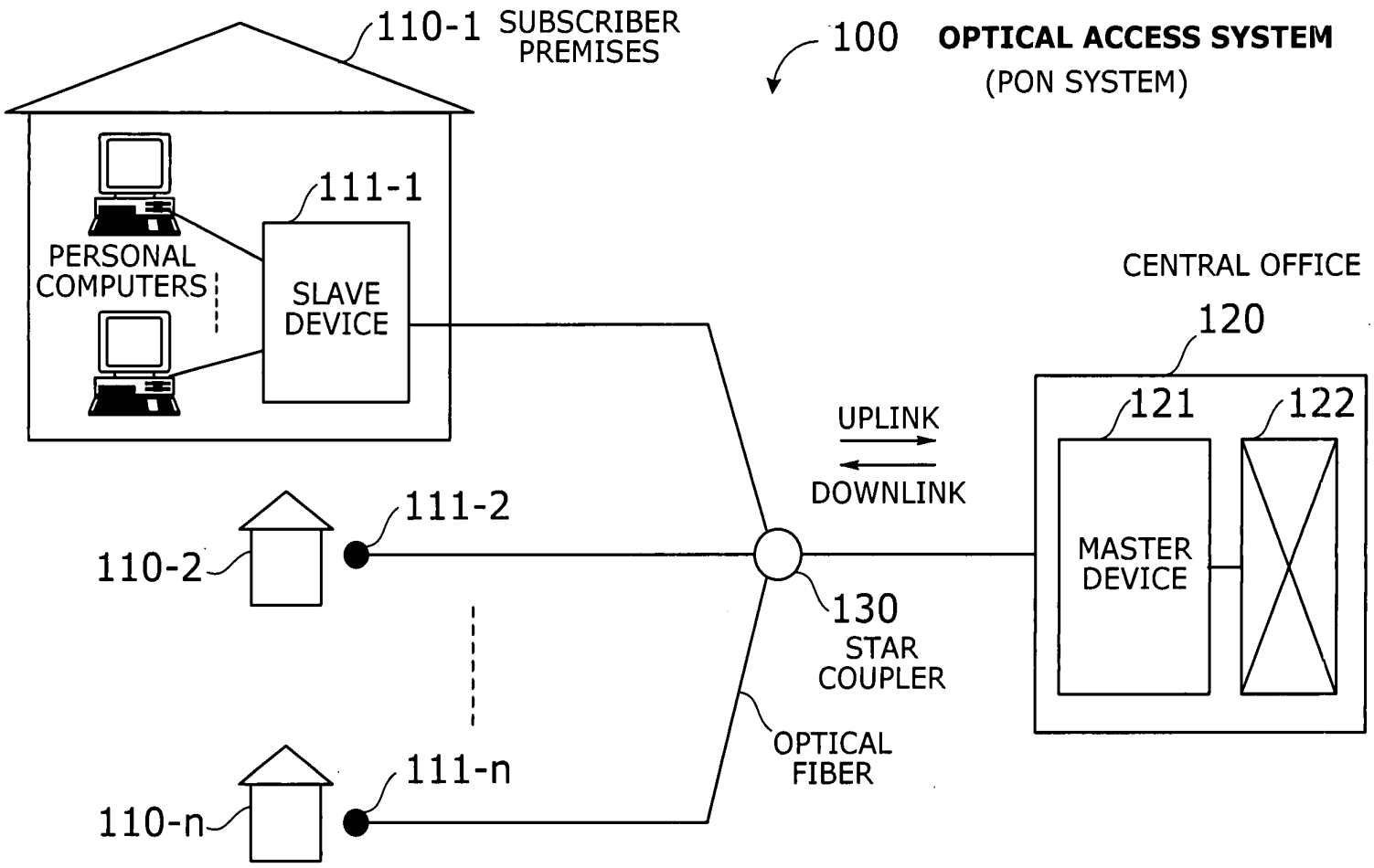


FIG. 25 *PRIOR ART*

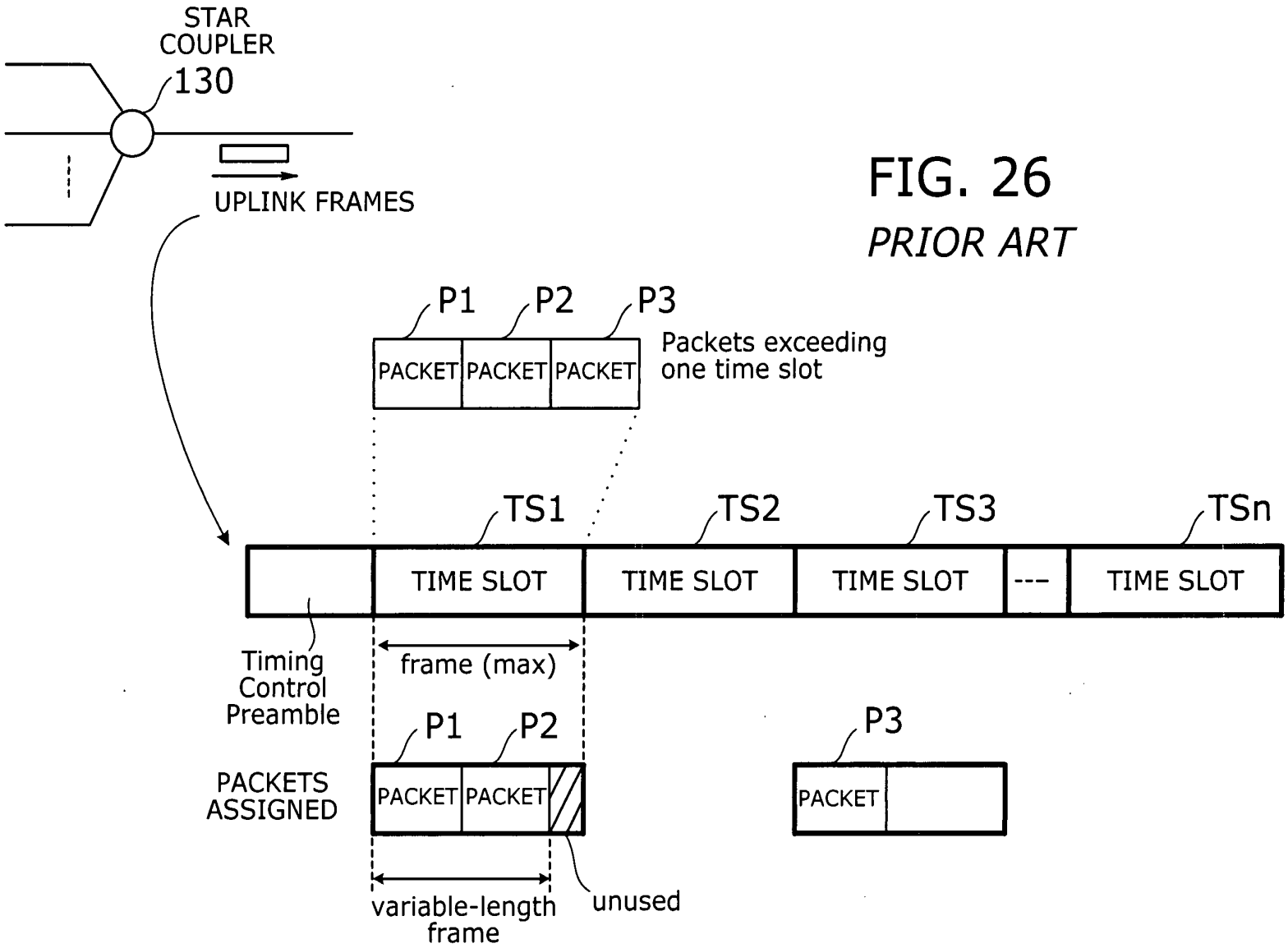


FIG. 26

PRIOR ART

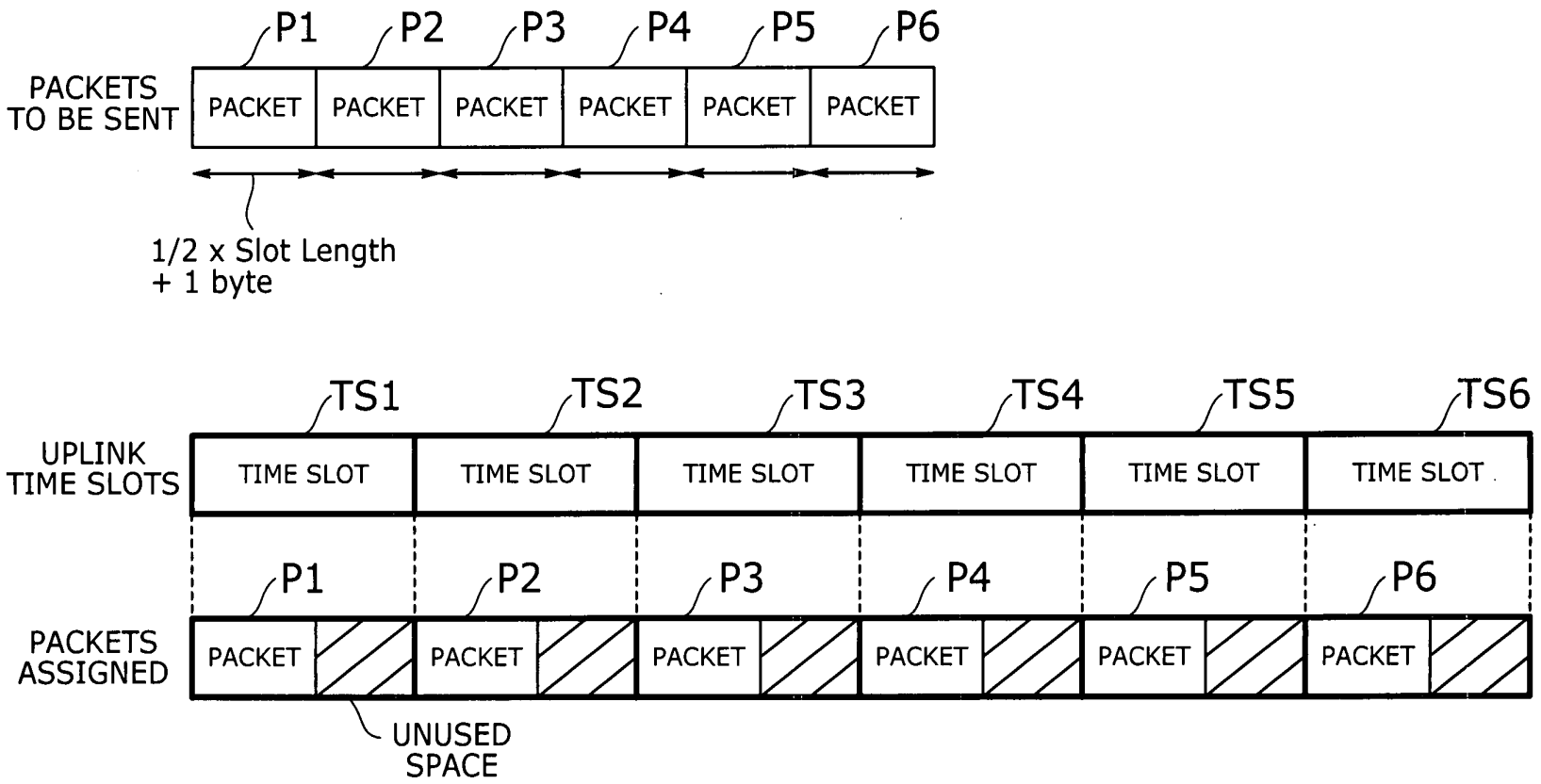


FIG. 27 *PRIOR ART*